SN74LS51N

■ Product Introduction

The SN74LS51N integrates a set of two-way two-input AND-OR-INVERT gates and a set of two-way three-input AND-OR-INVERT gates. The two gates are independent of each other.

■ Product Features

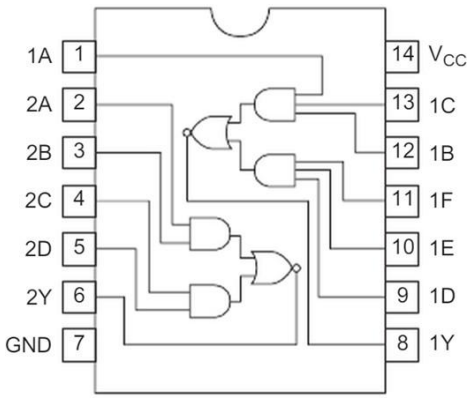
- Integrating two sets of multiple input AND-OR-NON gates
- Fully compatible with TTL/DTL input and output logic level
- Package : DIP14, SOP14

■ Product Applications

- Digital logic driver
- Industrial control applications
- Other application areasBattery-powered equipment

■ Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input 1A	14	Supply VCC
2	Input 2A	13	Input 1C
3	Input 2B	12	Input 1B
4	Input 2C	11	Input 1F
5	Input 2D	10	Input1E
6	Output 2Y	9	Input 1D
7	Supply GND	8	Output 1Y

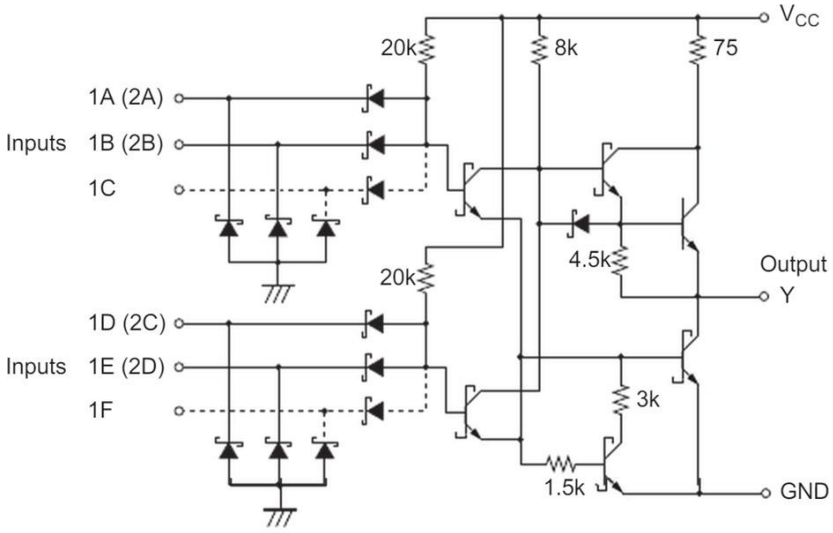


■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



$\overline{ABC + DEF} = Y$ $\overline{AB + CD} = Y$

Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IH}	2	—	—	V
	V_{IL}	—	—	0.7	V
Output current	I_{OH}	—	—	-400	uA
	I_{OL}	—	—	8	mA
Operating temperature	T_A	0	—	60	℃

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Output voltage	V_{OH}	2.7	3.3	-	V	I_{OH}=-400uA	VCC=4.75V, V_{IL}=0.7V
	V_{OL}	—	0.20	0.4	V	I_{OL}=4mA	VCC=4.75V, V_{IH}=2V
			0.35	0.5		I_{OL}=8mA	
Input current	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	0.24	0.4	mA	VCC=5.25V, V_I=0.4V	
Short-circuit output current	$I_{OS(Note1)}$	—	-15	-100	mA	VCC=5.25V	
Supply current	I_{CCH}	—	1.0	1.6	mA	VCC=5.25V, all V_I=GND	
	I_{CCL}	—	2.0	2.8	mA	VCC=5.25V, all V_I=VCC	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I=-18mA	

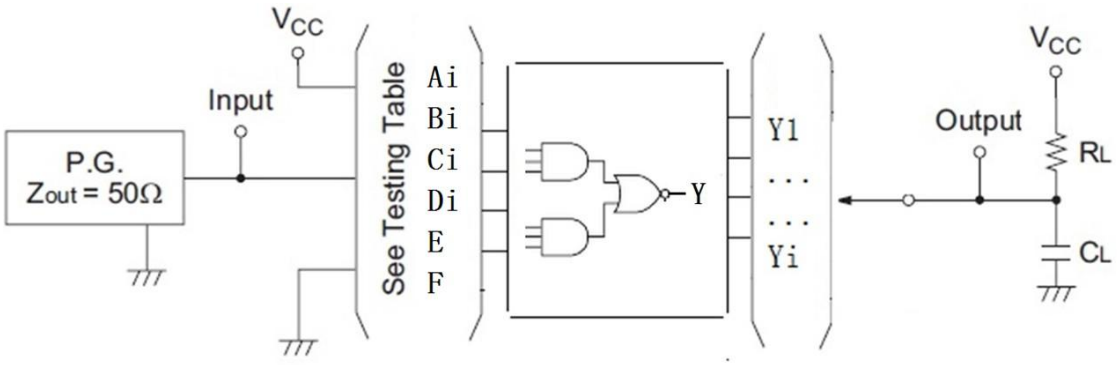
Note1: only one output port is short circuited each time, and the short circuit time is not more than one second.

■ Switching Characteristics (TA=25℃, Unless specified)

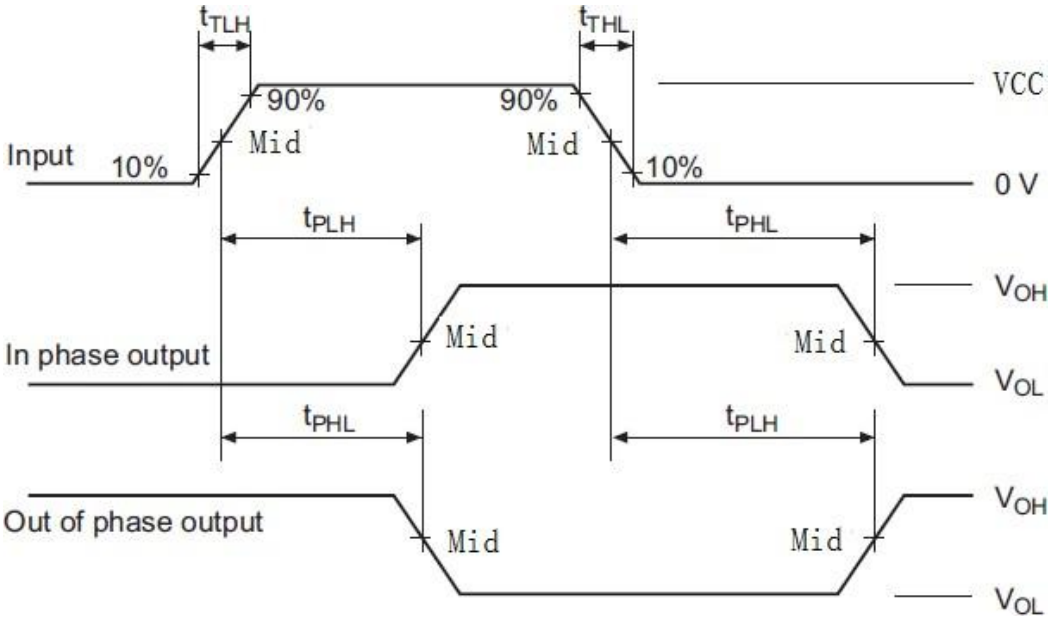
Item	Symbol	Min	Typ	Max	Unit	Conditions
Propagation delay time	t_{PLH}	—	30	—	ns	VCC=5V, CL=16pF, RL=2KΩ
	t_{PHL}	—	6	—	ns	

■ Testing Method

1、Test Circuit



2、Waveform



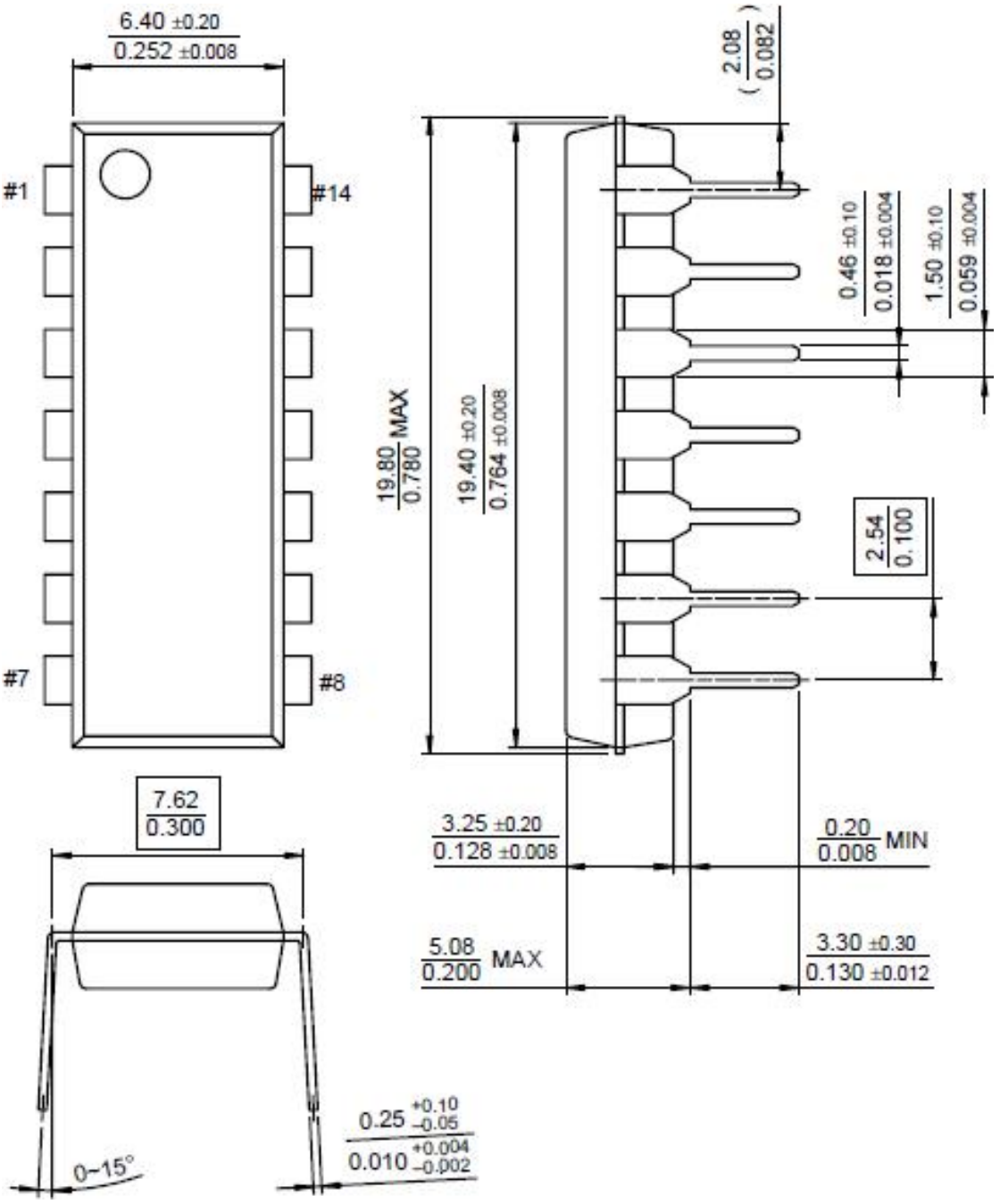
Note:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=1MHz, D=50%, tTLH=tTHL or less 20ns;
4. Output: Y output test port (Out of Phase Output, In Phase Output)

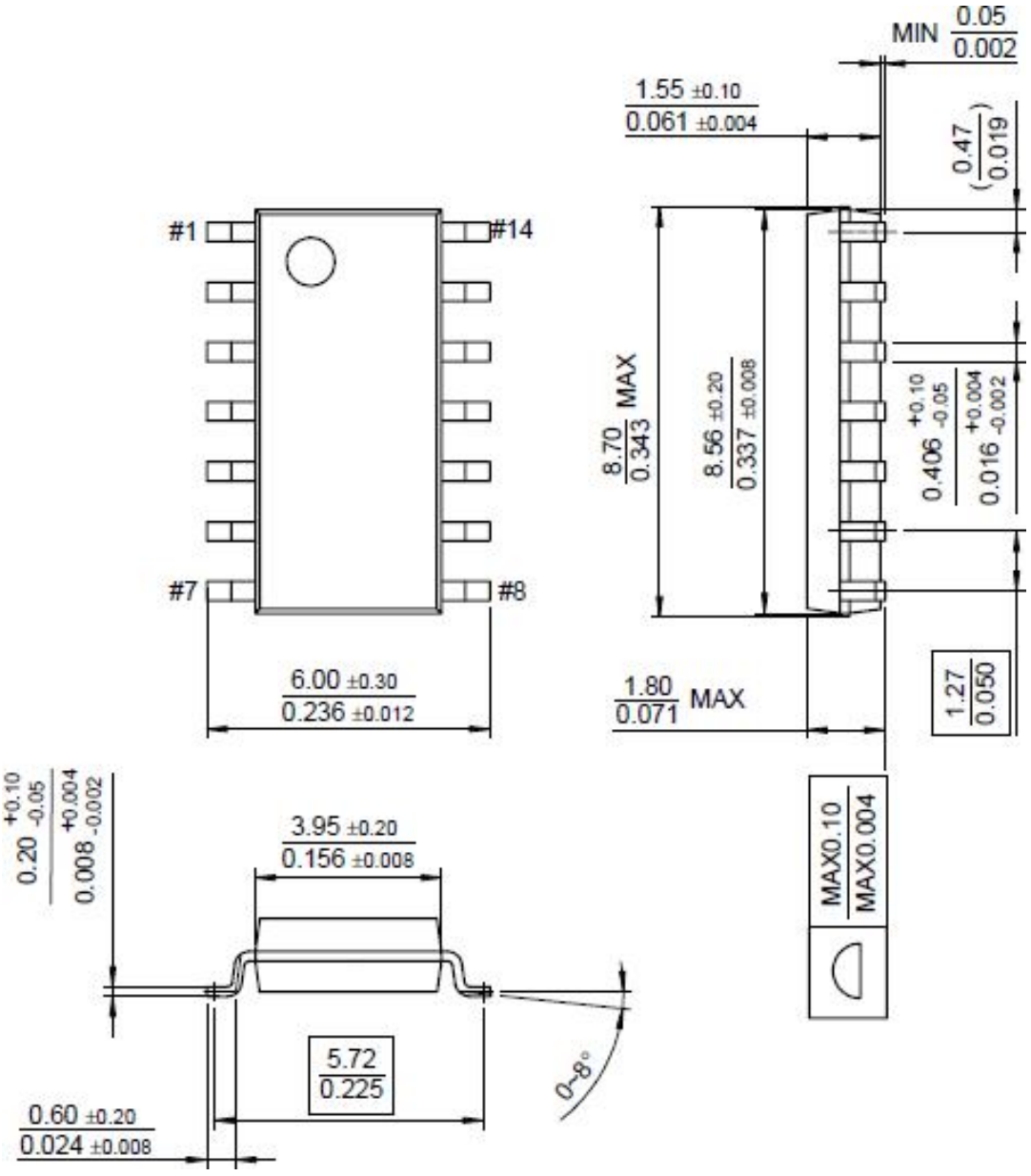
■ Package Dimensions

Unit : mm /inch

DIP14



SOP14


MIN 0.05 0.002
1.55 ±0.10
0.061 ±0.004
0.47 (0.019)
#1
#14
#7
#8
8.70 MAX 0.343
8.56 ±0.20 0.337 ±0.008
0.406 +0.10 -0.05
0.016 +0.004 -0.002
6.00 ±0.30
0.236 ±0.012
1.80 MAX 0.071
1.27 0.050
0.20 +0.10 -0.05
0.008 +0.004 -0.002
3.95 ±0.20
0.156 ±0.008
MAX0.10 MAX0.004
5.72 0.225
0~8°
0.60 ±0.20
0.024 ±0.008